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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,161	08/08/2005	Robert Giehrl	30051/41004	6490

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MARSHALL, GERSTEIN & BORUN LLP
233 SOUTH WACKER DRIVE
6300 SEARS TOWER
CHICAGO, IL 60606-6357

EXAMINER	
STEVENS, THOMAS H	
ART UNIT	PAPER NUMBER
2121	

MAIL DATE	DELIVERY MODE
01/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,161	GIEHRL ET AL.	
	Examiner	Art Unit	
	THOMAS H. STEVENS	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 13-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9,13-23 were examined.

Section I: Prosecution Reopened.

2. Based on applicants response 01/08/2009 that were completely responsive and acknowledged to the final office action. However based on the breath of the claims, prosecution is reopened with a new office action as set forth below.

Section II: Non-Final Rejection

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim1-9,13-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guignet (US Patent 5,734,572; Guignet) in view of Henley (US Patent 4,588,950; hereafter Henley). While Guignet teaches state variable associated with circuits, one of ordinary skill in the art of computer-based circuit analysis would want to improve said analysis program by incorporating visual access to the circuit. Henley teaches a method of displaying the logic levels in each segment of the circuit. Thus, at the time of invention it would have been obvious to one of ordinary skill in the art of computer-based circuit analysis to try to integrate the display capability and the integrated circuit since it would be easier to view (e.g., TV camera, figure 2, element 24) logic gate errors (Henley: column 1, line 23) in order to isolate a faulty instruction or set of instructions (Henley: column 1, lines 29-31). *(KSR International Co. v. Teleflex Inc., 550 USPQ2d 1385 (2007)).*

Claims 1-9 and 13-23 Guignet teaches

- represent at least one physical state variable (column 12, lines 36-38);
- circuit diagram (e.g., figure 11)

Claims 1-9 and 13-23 Henley teaches

- method for displaying data (figure 1, logic analyzer display)
- a machine control system (computer based machine control loop, figure 3)
- receiving status data (column 3, lines 16-21, in particular, line 17)
- at least one element of the system (e.g., A/D converter, figure 3)
- displays, at least for the element (figure 1, logic analyzer display)
- circuit diagram (e.g., figure 4A)
- an electrical connection (e.g., figure 4A) of the element to other individual elements
- which have been received for the element occurs in the represented (e.g., various stages of the IC, figure 1 element 14)

Per claim 2 Henley teaches

- connection data (plurality of nodes associated with each connection of the logic state, column 2, lines 48-60), which represent the electrical connection of the element in the system.

- Circuit characterization (column 2, lines 55-57)

Per claims 6,14,15 Henley teaches

- user input, (e.g. test engineer…isolate a faulty instruction or set of instructions, and from circuit diagrams the engineer can mark locations of the key nodes of interest on a layout, column 1, lines 29-32) which establishes a preset value

Per claims 7,16 Henley teaches

- target values (example of target values, figure 1, logic analyzer display)

Section II: Response to Argument

102(b)

6. Withdrawn.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure:

- US 7356786 discloses the ability to debug hardware designs at the HDL level facilitates correction or adjustment of the HDL description of the hardware designs.
- US 6151689 discloses a multiprocessor system includes a number of sub-processor systems, each substantially identically constructed, and each comprising a central processing unit (CPU), and at least one I/O device, interconnected by routing apparatus that also interconnects the sub-processor systems.
- US 5675808 discloses a power control and memory refresh rate management circuit is described.
- US 7072818 discloses the ability to debug hardware designs at the HDL level facilitates correction or adjustment of the HDL description of the hardware designs.
- US 4588950 discloses a conductive state of a transistor in a semiconductor integrated circuit is determined by irradiating the transistor with a radiation beam and measuring changes in load current, thereby indicating whether the transistor was conducting or non-conducting prior to irradiation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715.

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Albert Decady (571-272-3819). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

/Albert Decady /
Supervisory Patent Examiner
Tech Center 2100

/Thomas H. Stevens/

Examiner, Art Unit 2121